RSoC Framework

www.rsoc-framework.com

Video demonstration

Application Note

Version 1.1
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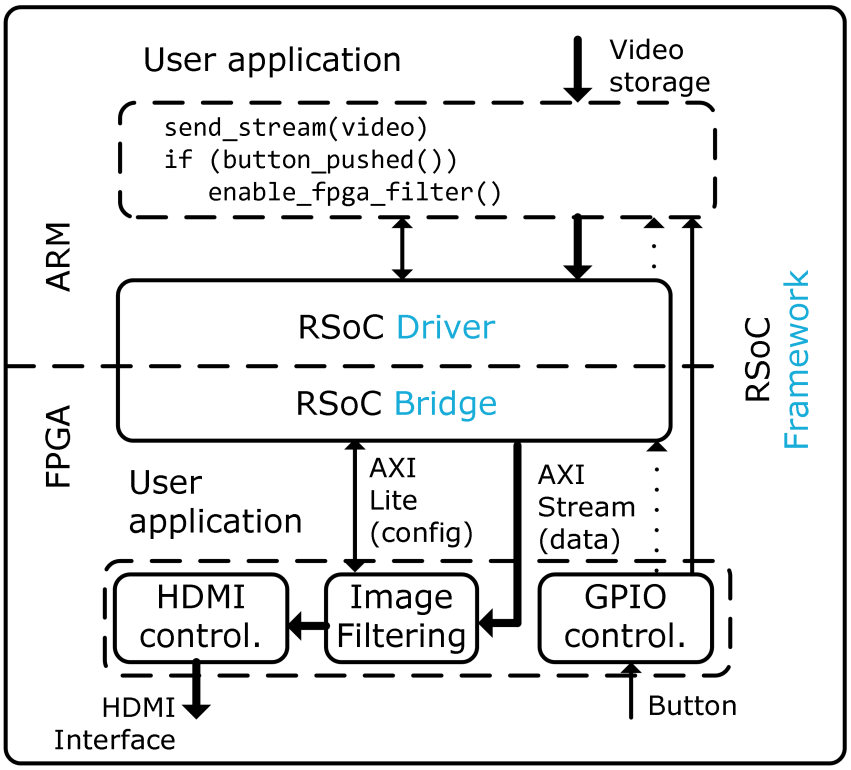
Introduction

The goal of this document is to describe contents of the Video demonstration application based on the RSoC Framework for Zynq. The application consists of FPGA and processor parts. The FPGA part is used to accelerate median filter and to deliver video data to HDMI output interface. The processor controls sending of data. The demonstration works on Zedboard, however, it may be ported to another board by changing the design pinout. After reading this document the reader is expected to understand the architecture of the demonstration and to be able to modify both the software and hardware parts of the application.



Requirements

The demonstration is prepared for Avnet Zedboard with a screen connected by HDMI. A quick start guide for Zedboard can be found at `http://zedboard.org/support/documentation/1521`.

Contents of demonstration

The demonstration can be downloaded from `rsoc-framework.com/files/video_demo_bin.zip`

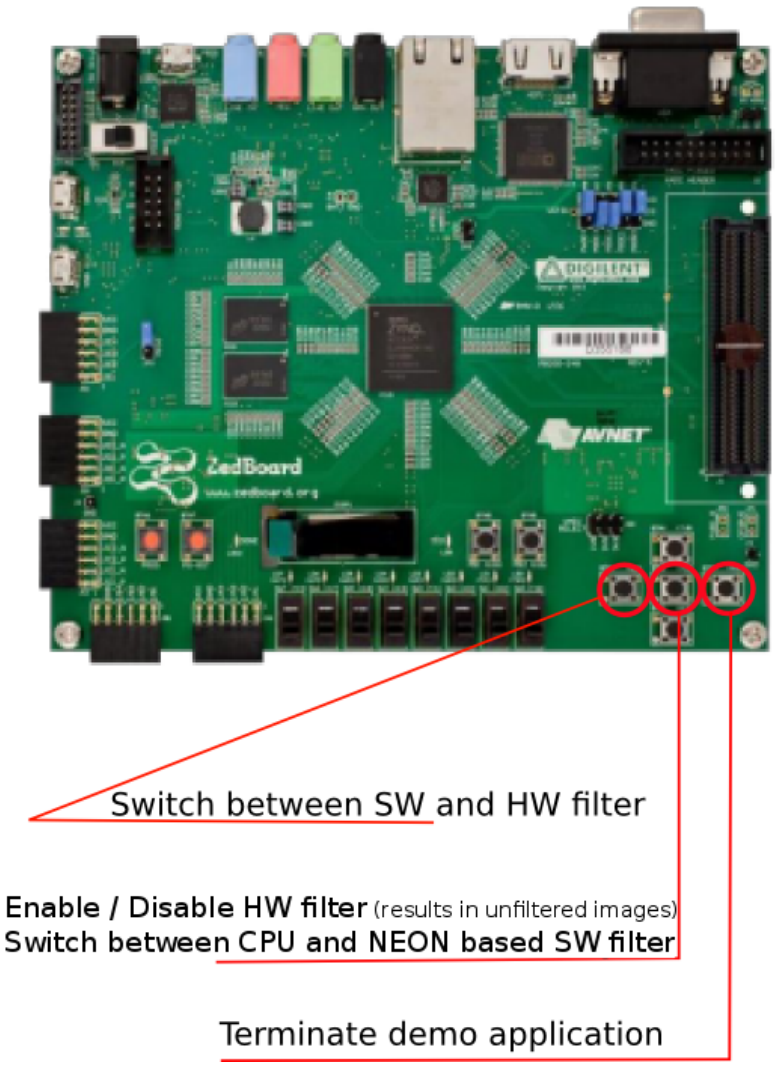
Quick start

Connect the HDMI output of ZedBoard to monitor capable of resolution 1280x720x60Hz.

To quickly test the application, copy the following files to the Zedboard's SD card:

- `uramdisk.image.gz` filesystem,
- `uImage` the Linux Kernel,
- `devicetree.dtb` device-tree describing the hardware and FPGA firmware,
- `BOOT.BIN` Zynq specific bootloader and FPGA design.
- `video` Directory with video images.

Boot Zedboard (takes about a minute) with the SD card prepared in the previous step. You should see a video on the screen. It is possible to enable/disable the integrated hardware median filter by pressing button BTNL. It is also possible to switch between CPU and NEON software median filter implementations by pressing button BTNC. To reboot the demonstration, use button PS-RST (BTN7).



Software application sources

The application sources can be downloaded from `rsoc-framework.com/files/video_demo_sw.zip`

The video demo application consists from following sources:

+ `video_demo.c` Main source code, contains main execution loop.
+ `sw_filter.c` Implementation of software 3x3 median filter. The filter is executed in separate thread. Median filter is implemented by sorting network. There are two implementations of the median filter. One is based on ARM CPU core and the other is based on ARM NEON SIMD engine.
+ `load_image.c` Implementation of video image loading. Uses image library stb_image.
+ `stb_image.c` Public domain image library.
+ `rsoc_hal.c` Hardware abstraction layer (HAL) of RSoC Framework. The HAL abstracts low level implementation of DMA transfers, configuration and buffer allocation. The HAL is specific for this demo application.
+ `zed_buttons.c` Functionality for reading events sent by push buttons on ZedBoard. Module gpio_keys must be loaded or compiled in the kernel.

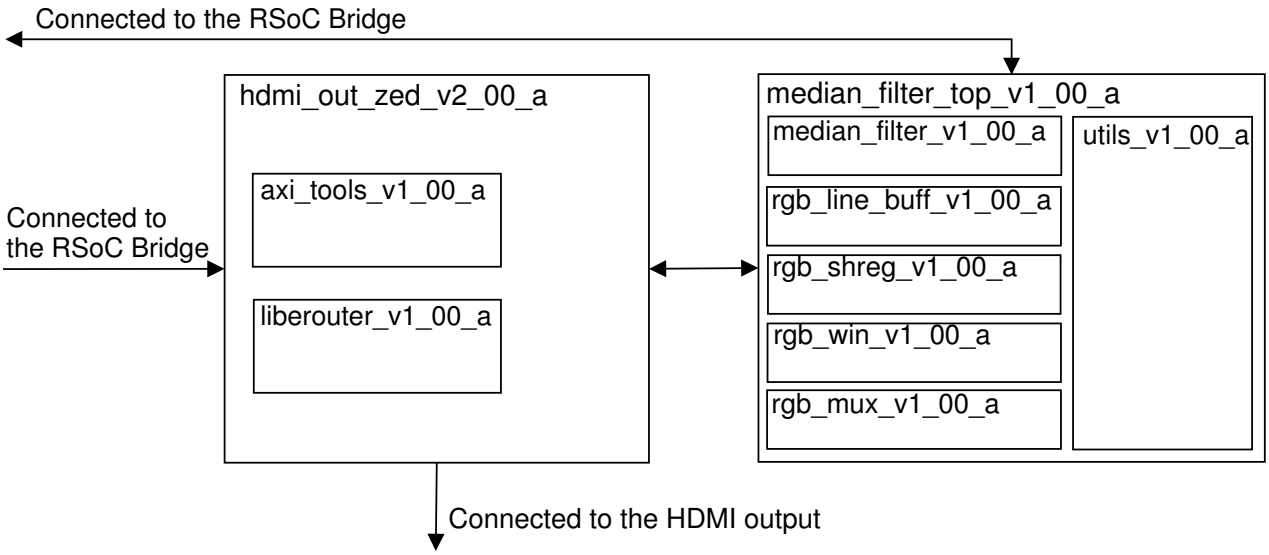
The video demo application depends on dynamic libraries libpthread and libaio. The package is intended for integration with the buildroot environment.

Firmware (FPGA) application sources

The application sources can be downloaded from `rsoc-framework.com/files/video_demo_fw.zip`

The video demo application FPGA components consist of following directories:

+ `hdmi_out_zed_v2_00_a` HDMI output for ZedBoard for EDK and Vivado
+ `axi_tools_v1_00_a` Package used by HDMI output component
+ `liberouter_v1_00_a` Package used by HDMI output component
+ `median_filter_top_v1_00_a` Implementation Median filter for EDK and Vivado
+ `median_filter_v1_00_a` Package used by Median filter component
+ `rgb_line_buff_v1_00_a` Package used by Median filter component
+ `rgb_mux_v1_00_a` Package used by Median filter component
+ `rgb_shreg_v1_00_a` Package used by Median filter component
+ `rgb_win_v1_00_a` Package used by Median filter component
+ `utils_v1_00_a` Package used by Median filter component
+ `demo.ucf` UCF constraints for EDK
+ `demo.xdc` XDC constraints for Vivado



Customization of application

The software and firmware application sources can be freely modified to suit your needs. The only other component needed to build the design is the RSoC Framework. The trial version of the RSoC Framework can be obtained from `info@rsoc-framework.com` free of charge.